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Question Paper Code : 80441

B.E./B.Tech DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Third Semester

Electronics and Communication Engineering

EC 2205/EC 36/080290011 – ELECTRONIC CIRCUITS – I

(Regulations 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Define stability factor.

2. What are the different methods of biasing JFET?

3. Draw the small signal equivalent circuit of CE amplifiers.

4. State Bisection theorem.

5. Define Gain Bandwidth product.

6. Draw the high frequency equivalent circuit of FETs.

7. Define conversion efficiency of power amplifier.

8. What is cross over distortion in class B power amplifier?

9. Define ripple factor of a rectifier.

10. What is the function of a current limiting circuit?

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Draw the circuit of a voltage divider bias circuit. Explain its operation and discuss how it stabilizes against V_{BE} changes. (8)

(ii) Derive the stability factor of the voltage divider bias circuit. Compare the stability factor of fixed bias and voltage divider bias circuits with h_{FE} = 100, R_e = I Kohm, R_1 = 33Kohm and R_2 = 12 Kohms. (8)

Or

(b) (i) Explain the circuit of gate bias for Providing stabilization of JFET. (8)

(ii) Sketch the bias circuit for enhancement MOSFETS and explain its operation. (8)

12. (a) (i) Compute the parameters of the circuit shown in Figure 12(a) with $\beta = 100$. (10)

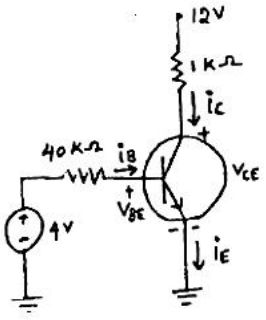

Figure 12(a)

(ii) Explain in detail about the Miller's theorem. (6)

Or

(b) Compare CE, CB and CC transistor configurations

(i) In terms of input impedance output impedance current gain and voltage gain. (10)

(ii) Draw the output characteristics of CE configuration and mark its regions of operation. (6)

13. (a) (i) Draw the high frequency hybrid π model for a transistor in the CE configuration and explain the significance of each component. (12)

(ii) Define alpha cut off frequency. (4)

Or

(b) (i) Define the frequency response of multistage amplifier and derive its upper and lower cut-off frequencies. (8)

(ii) How does Rise and Sag time related to cut-off frequencies? Justify. (8)

14. (a) (i) Derive the relation between rise time and upper 3 db frequency of an amplifier. (10)

(ii) Four identical stages are cascaded. The lower and Upper 3 dB frequencies of each stage are 40 Hz and 20 KHz respectively. Calculate the overall bandwidth of the cascaded amplifier (6)

Or

(b) Derive expression for upper and lower cutoff frequencies of a capacitively coupled multistage amplifier. (16)

15. (a) (i) In a full wave rectifier a signal of 300 volts at 50 Hz is applied at the input. Each diode has an internal resistance of 800 Ω. If the load is 2000 ohms calculate

(1) Instant peak value of current in the output, (3)

(2) Output de current and, (3)

(3) Efficiency of power transfer. (3)

(ii) Explain about voltage multipliers. (7)

Or

(b) Explain the following:

(i) Switched Mode Power Supply (SMPS) (8)

(ii) Power control using SCR. (8)

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